IN THE SPECIFICATION:

Please replace paragraph **[00107]** with the following:

[00107] Signal generator 2102 asserts enable signals on signal lines 2103_A and 2103_B at approximately the same time that comparand register 208 outputs comparand data on the comparand signal lines CL and $\overline{CL}$ to each of the subarrays. When the dynamic timing generator 220_A and 220_B receive their asserted enable signals on signal lines 2103_A and 2103_B respectively, dynamic timing generator 220_A outputs its latch enable signal on signal line 203_A to latches 202_1-202_X and dynamic timing generator 220_B outputs its latch enable signal on signal line 203_B to latches 202_{X+1}-202_K. For an alternative embodiment, the enable signals on signal lines 2103_A and 2103_B enable the dynamic timing generators to start their operations. Since the dynamic timing generators will not assert their latch enable signals until after their respective subarrays have received their comparand data and ~~has~~ have commenced their compare operations, the latch enable signals on signal lines 203_A and 203_B will cause latches 202_1-202_K to capture the correct match results for a given compare operation.